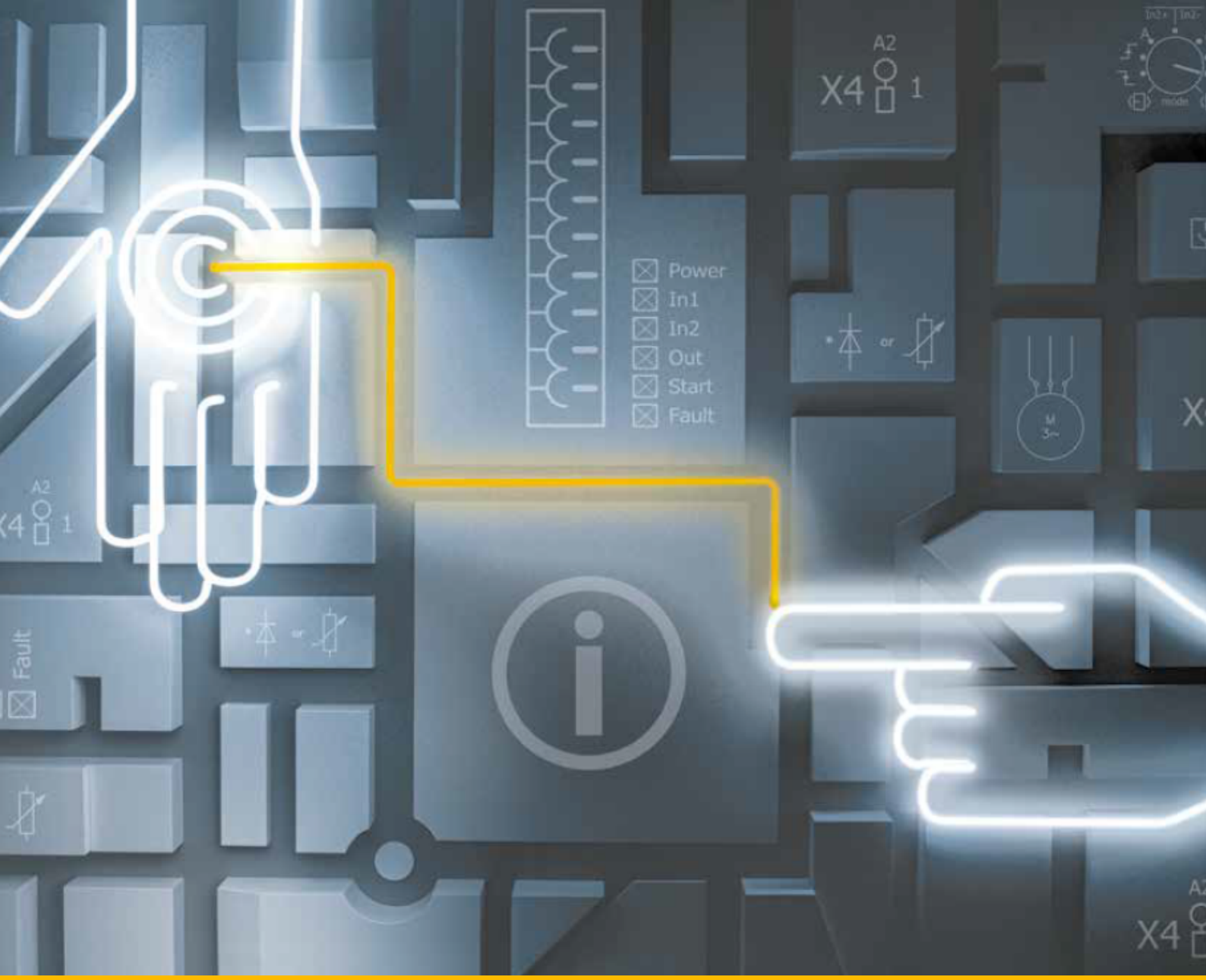

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Intel MPL 17.0

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>>>>>>>>>>>>>> Intel (Altera) MPL (Minimal Preloader) <<<<<<<<<<<<<

Summary:

The Minimal Preloader (MPL) is an alternative for the GPL Preloader. It uses the BSD license and may be freely distributed and modified according to the terms of that license. The MPL supports a subset of features supported by Altera's GPL Preloader.

The MPL initializes the PLLs, reset signals, configures IOCSR and pinmuxing and performs other configuration based on the preloader generator file settings. It can also load the FPGA from a boot source if desired. It then reads a secondary image from a boot source into RAM and hands control to that image.

This version of MPL supports booting from QSPI, SDMMC, NAND and FPGA. Most of the MPL testing used CSEL set to 0. Other CSEL settings may work but are not tested.

For SDMMC, you may put the secondary image on a FAT partition or on the raw partition that contains the MPL image. For loading the FPGA in this case, the secondary image and the FPGA image must both be on the FAT partition.

The MPL uses Altera HWLib drivers for most of its functionality. It also uses Altera HWLib SoCAL folders for the memory map definitions and basic read/write commands.

The MPL supports both the ARMCC and GNU GCC compilers. The MPL supports Cyclone V (CV), Arria V (AV), & Arria 10 (A10) SoC devices. The example commands shown in this file are for Cyclone V SoC. Please modify the examples as needed to select appropriate file names.

For Arria 10, UEFI provides a full-featured bootloader and is the preferred non-GPL method of booting the SoC. The MPL provides a minimal set of functionality and should be considered by those wanting a basic loader, or a small application to do chip initialization.

You can find more information about UEFI for Arria 10 here:

http://www.altera.com/en_US/pdfs/literature/ug/ug-a10-soc-boot.pdf

http://github.com/altera-opensource/uefi-socfpga

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uum_malloc 1.1.2

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